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EXAMINER	
MCFADDEN, MICHAEL B	

ART UNIT	PAPER NUMBER
2188	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/691,137	ROBOTHAM, ROBERT ELLIOTT	
	Examiner	Art Unit	
	Michael B. McFadden	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-5* is/are allowed.

6)☒ Claim(s) *6-19* is/are rejected.

7)☒ Claim(s) *20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

1. Claims 1-20 are pending in the Application.

Response to Amendment

2. Applicant's arguments filed on 05 June 2006 have been fully considered but they are not persuasive.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 6, 7, 10, 11, 14, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ukai et al. ((U.S. Patent No. 5,809,516) herein after Ukai).

a. **As per claim 6**, Ukai discloses a method comprising:

accessing within one memory access operation **(column 4, lines 48-53)** a plurality of storage devices **(Figure 1, element 4 and column 8, lines 28-29)** such that a first portion of the plurality of storage devices is accessed at a first hardware memory address and a second portion of the plurality of storage

devices is accessed at a second hardware memory address adjacent to the first hardware memory address **(Figure 38 and column 29, lines 53-56).**

The reference shows a RAID Level 5 disc array that shows the logical blocks of memory are allocated adjacent to each other and are accessed concurrently (in parallel).

b. **As per claim 7**, Ukai discloses the method of claim six wherein the plurality of storage devices are separate storage devices **(Figure 1, element 4, drives #D0, #D1, #D2, #D3, #D4 and column 8, lines 28-29)** with respectively separate address buses **(Figures 1, 18, 24, and 32)**.

Note that Figures 1, 18, 24, and 32 show that four drives are accessed separately using a different bus. Furthermore note that inherently, each bus includes an address control and data lines.

c. **As per claim 10**, Ukai discloses a system comprising:

a first storage device **(Figure 1, element 4, drive #D0)**;

a second storage device **(Figure 1, element 4, drive #D1)**; and

a processor **(Figure 1, element 1 and column 8, lines 36-39)** coupled to the first storage device and to the second storage device , the processor configured to access within one memory access operation **(column 4, lines 48-53)**, a first hardware memory address of the first storage device and a second hardware memory address of the second storage device, the second hardware memory address being adjacent to the first hardware memory address**(Figure 38 and column 29, lines 53-56)**.

Note that Figure 1 discloses a host (i.e. processor) that issues requests to the disk drives.

The reference shows a RAID Level 5 disc array that shows the logical blocks of memory are allocated adjacent to each other and are accessed concurrently (in parallel)

d. **As per claim 11**, Ukai discloses the system of claim 10 wherein the first storage device and the second storage device are separate storage devices **(Figure 1, element 4, drives #D0, #D1 and column 8, lines 28-29)** provided with respectively separate address buses **(Figures 1, 18, 24, and 32)**.

Note that Figures 1, 18, 24, and 32 show that four drives are accessed separately using a different bus. Furthermore note that inherently, each bus includes an address control and data lines.

e. **As per claim 14**, Ukai discloses a memory system comprising:
A plurality of memory banks **(Figure 1, element 4 and column 8, lines 28-29)** accessible via a plurality of modes of access **(column 4, lines 19-22 and column 4, lines 48-49)** to allow selection **(column 28, lines 16-24)** among a plurality of predefined memory access starting points **(Figure 37 and column 27, lines 61-63)**, wherein the predefined memory access starting points occur at intervals of less than a total memory bandwidth **(Figure 37 and column 4, lines 48-53)**.

The "plurality of modes of access" is demonstrated by the read and write functionality of the disk drives disclosed in Ukai.

The write operation allows selection when the disk drive to perform the present write request is selected. The disk is selected in a way that the prior write request will not interfere with running both requests in parallel. It should also be noted that the different disk drives are allocated into a plurality of memory banks. By being able to write to and select each bank it demonstrates the capability of selection.

A "plurality of predefined memory access starting points" is shown in the plurality of banks shown in Figure 37. In column 4, lines 48-53 Ukai states that it is possible to read all of the drives that are connected in parallel. This would then mean that the total memory bandwidth of the system is, in this embodiment, five blocks and the predefined starting points occur every block, therefore occurring at intervals that are less than the total memory bandwidth.

f. **As per claim 19**, Ukai discloses the memory system of claim 14 wherein an amount of desired data is stored contiguously within a system memory address space of the memory system **(Figure 38 and column 29, lines 53-56)**.

The reference shows that the blocks are allocated in a contiguous fashion and that data would be stored in that manner.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 8, 9, 12, 13, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ukai et al. ((U.S. Patent No. 5,809,516) herein after Ukai) as applied to claims 6, 10, and 14 above, and further in view of Yokote et al. ((U.S. Patent No. 5,651,129) herein after Yokote).

a. **As per claim 8**, Ukai fails to disclose the method of claim 6 wherein the plurality of storage devices are implemented within a larger storage device, the larger storage device comprising an input to select an addressing mode.

Yokote discloses wherein the plurality of storage devices **(Figure 2, element 26 and column 3, lines 18-20)** are implemented within a larger storage device **(Figures 1 & 2, element 16 and column 3, lines 18-20)**, the larger storage device comprising an input to select an addressing mode **(Figure 2, element 24 and column 3, lines 24-32)**.

Yokote discloses a controller/memory module that is a memory controller, which controls an array of DRAM chips. The controller has multiple input buses in order to determine the location and type of memory access to occur. The controller is able to process read and write instructions, and thereby fulfills the requirement of multiple addressing modes.

Ukai and Yokote are analogous art because they are from the same field of endeavor, mass data storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai **(Figure 1, element 4)** with the controller/memory modules of Yokote **(Figure 1, element 16).**

The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage **(Yokote - column 1, lines 54-57)**.

Therefore, it would have been obvious to combine the controller/memory module of Yokote with the mass storage device of Ukai for the benefit of a mass storage device providing high-density, high-capacity storage to obtain the invention as specified in claim 8.

b. **As per claim 9**, Ukai fails to disclose the method of claim 8 wherein the addressing mode allows selection of different hardware memory addresses among the plurality of storage devices for a same memory access operation.

Yokote discloses the method of claim 8 wherein the addressing mode allows selection of different hardware memory addresses **(column 3, lines 24-32)** among the plurality of storage devices for a same memory access operation **(column 3, lines 48-54)**.

Yokote discloses the memory controller containing multiple buses, which provide multiple access modes to access memory. Included in these buses are a read data bus, a read address bus, a write data bus, a write

address, and a control bus. The read address bus and the write address are both capable of handling references to memory addresses, therefore allowing selection of different hardware memory addresses.

The controller/memory modules have the ability to access, in parallel, multiple DRAM chips in the 8x4 array. Accessing in parallel is accessing multiple memories concurrently, in other words, in one memory access operation.

Ukai and Yokote are analogous art because they are from the same field of endeavor, mass data storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai **(Figure 1, element 4)** with the controller/memory modules of Yokote **(Figure 1, element 16).**

The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage **(Yokote - column 1, lines 54-57)**.

Therefore, it would have been obvious to combine the controller/memory module of Yokote with the mass storage device of Ukai for the benefit of a mass storage device providing high-density, high-capacity storage to obtain the invention as specified in claim 9.

c. **As per claim 12**, Ukai fails to disclose the system of claim 10 wherein the first storage device and the second storage device are implemented within a

larger storage device, the larger storage device comprising an input to select an addressing mode.

Yokote discloses wherein the first storage device and the second storage device **(Figure 2, element 26 and column 3, lines 18-20)** are implemented within a larger storage device **(Figures 1 & 2, element 16 and column 3, lines 18-20)**, the larger storage device comprising an input to select an addressing mode **(Figure 2, element 24 and column 3, lines 24-32)**.

Yokote discloses a controller/memory module that is a memory controller, which controls an array of DRAM chips. The controller has multiple input buses in order to determine the location and type of memory access to occur. The controller is able to process read and write instructions, and thereby fulfills the requirement of multiple addressing modes.

Ukai and Yokote are analogous art because they are from the same field of endeavor, mass data storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai **(Figure 1, element 4)** with the controller/memory modules of Yokote **(Figure 1, element 16).**

The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage **(Yokote - column 1, lines 54-57)**.

Therefore, it would have been obvious to combine the controller/memory module of Yokote with the mass storage device of Ukai for the benefit of a mass storage device providing high-density, high-capacity storage to obtain the invention as specified in claim 12.

d. **As per claim 13**, Ukai fails to disclose the system of claim 12 wherein the addressing mode allows selection of different hardware memory addresses among the first storage device and the second storage device for a same memory access operation.

Yokote discloses the system of claim 12 wherein the addressing mode allows selection of different hardware memory addresses **(column 3, lines 24-32)** among the first storage device and the second storage device for a same memory access operation**(column 3, lines 48-54)**.

Yokote discloses the memory controller containing multiple buses, which provide multiple access modes to access memory. Included in these buses are a read data bus, a read address bus, a write data bus, a write address, and a control bus. The read address bus and the write address are both capable of handling references to memory addresses, therefore allowing selection of different hardware memory addresses.

The controller/memory modules have the ability to access, in parallel, multiple DRAM chips in the 8x4 array. Accessing in parallel is accessing multiple memories concurrently, in other words, in one memory access operation.

Ukai and Yokote are analogous art because they are from the same field of endeavor, mass data storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai **(Figure 1, element 4)** with the controller/memory modules of Yokote **(Figure 1, element 16).**

The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage **(Yokote - column 1, lines 54-57)**.

Therefore, it would have been obvious to combine the controller/memory module of Yokote with the mass storage device of Ukai for the benefit of a mass storage device providing high-density, high-capacity storage to obtain the invention as specified in claim 13.

e. **As per claim 17**, Ukai fails to disclose the system of claim 14 wherein the predefined memory access starting points occur in the memory banks as a function of a size of a desired data block to be accessed.

Yokote discloses the system of claim 14 wherein the predefined memory access starting points occur in the memory banks **(Figure 2)** as a function of a size of a desired data block to be accessed **(Column 2, lines 50-62)**.

Yokote discloses a system that can be configured to accommodate any required storage size. Yokote also discloses the use of an asynchronous transfer mode (ATM). When using an asynchronous transfer mode, data is transferred in units called cells. The cells are of fixed size

and format. Although not explicitly stated, the Examiner respectfully asserts that the system Yokote teaches is designed to utilize ATM cells, and therefore is designed to accommodate the usage of a storage unit of ATM cell size.

Ukai and Yokote are analogous art because they are from the same field of endeavor, mass data storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai **(Figure 1, element 4)** with the controller/memory modules of Yokote **(Figure 1, element 16).**

The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage **(Yokote - column 1, lines 54-57)**.

Therefore, it would have been obvious to combine the controller/memory module of Yokote with the mass storage device of Ukai for the benefit of a mass storage device providing high-density, high-capacity storage to obtain the invention as specified in claim 17.

f. **As per claim 18**, Ukai fails to disclose the memory system of claim 17 wherein the amount of desired data is an asynchronous transfer mode (ATM) cell.

Yokote discloses the memory system of claim 17 wherein the amount of desired data is an asynchronous transfer mode (ATM) cell. **(Figure 1, element 14 and Column 2, lines 59-62).**

Yokote teaches the use of an asynchronous transfer mode (ATM) switch. The use of an ATM switch would imply the use of an asynchronous transfer mode. In the use of an asynchronous transfer mode the data is stored in units called cells. These ATM cells are of fixed size and format. Therefore, although not explicitly stated, the Examiner respectfully asserts that the use of an ATM switch includes the use of an asynchronous transfer mode and an ATM cell.

Ukai and Yokote are analogous art because they are from the same field of endeavor, mass data storage devices.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai **(Figure 1, element 4)** with the controller/memory modules of Yokote **(Figure 1, element 16).**

The motivation for doing so would have been to create a mass data storage device providing high-density, high-capacity storage **(Yokote - column 1, lines 54-57)**.

Therefore, it would have been obvious to combine the controller/memory module of Yokote with the mass storage device of Ukai for the benefit of a mass storage device providing high-density, high-capacity storage to obtain the invention as specified in claim 19.

7. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ukai et al. ((U.S. Patent No. 5,809,516) herein after Ukai) as applied to claim 14 above, and further in view of McClure (U.S. Patent No. 5,590,307).

As per claim 15, Ukai fails to disclose the memory system of claim 14 wherein the plurality of memory banks are accessible via burst access.

McClure discloses the memory system of claim 14 wherein the plurality of memory banks are accessible via burst access **(Column 4, lines 13-15)**.

Ukai and McClure are analogous art because they are from the same field of endeavor, memory systems.

At the time of invention it would have been obvious to a person of ordinary skill in the art to replace the disk drives of Ukai with the **data cache placed in burst mode (Column 4, lines 13-15)** of McClure.

The motivation for doing so would have been to quickly transfer a line or lines of data. **(Column 4, lines 9-10)**

Therefore it would have been obvious to combine the data cache placed in burst mode of McClure with the memory system of Ukai for the benefit of quickly transferring a line or lines of data to obtain the invention as specified in claim 15.

8. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ukai et al. ((U.S. Patent No. 5,809,516) herein after Ukai) and McClure (U.S. Patent No. 5,590,307) as applied to claim 15 above, and further in view of Koutsoures (U.S. Patent No. 6,457,075).

As per claim 16, Ukai and McClure fail to disclose the memory system of claim 15 wherein the total memory bandwidth is equal to the burst size.

Koutsoures discloses the memory system of claim 15 wherein the total memory bandwidth is equal to the burst size **(Column 2, lines 44-46).**

Koutsoures refers to setting the cache line length equal to the burst size. The cache line length would be the total memory bandwidth because the memory system cannot transfer more data than the cache line can transfer.

Ukai, McClure, and Koutsoures are analogous art because they are from the same field of endeavor, memory systems.

At the time of the invention it would have been obvious to a person of skill in the art to set the burst length equal to the cache line length **(Column 2, lines 44-46).**

The motivation for doing so would have been to receive a complete line in response to a single address request **(Column 2, lines 44-46)**.

Therefore it would have been obvious to combine the idea of setting the burst length equal to the cache line length of Koutsoures with the memory system of Ukai and McClure for the benefit of receiving a complete line in response to a single address request to obtain the invention as specified in claim 16.

Allowable Subject Matter

9. Claims 1-5 are allowable over the prior art of record.

10. Claim 20 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

a. **As per claim 1,** Pogue et al. (U.S. Patent No. 4,920,483) teaches a parallel memory system for accessing a word-sized group of bits of any size. Also Pogue et al. teaches a processor connected to memory which determines the size of the memory. However, Pogue et al. does not teach a method for calculating the size of the group of bits, and therefore does not arrive at the limitations as claimed by the Applicant.

b. Baker et al. (U.S. Patent No. 5,144,692 and U.S. Patent No. 5,363,497) teach a parallel memory BCU logic system that divides data into 64 byte blocks of memory. Baker et al. does not disclose the use of a function to divide the memory blocks.

c. Sokolov (U.S. Patent No. 5,966,726 and U.S. Patent No. 5,890,213) discloses a disk drive with a chache memory unit that is divisible into a number of segments, each having a unique access type. The calculation to determine the size of the segments uses a number of factors. However, these factors are not the factors used by the Applicant in determining the

number of quantum to create. Also, it should be noted that Sokolov does not disclose multiple memories working in parallel.

d. Coleman et al. (U.S. Patent No. 5,440,687) teaches a parallel memory system that uses a recursive type function where data is stored one stride at a time until all data is stored in consecutive memory locations. Coleman et al. also makes note of the need for calculating a proper memory increment. However, Coleman et al. does not disclose an equation to achieve this objective.

e. DeMoss et al. (U.S. Patent No. 5,778,411) discloses a parallel memory system with a method to detect overflow. If the data to be stored exceeds the storage capacity for one unit, then another unit is designated for the remainder of the data. DeMoss et al. fails to disclose the use of a function in determining the size of memory allocations, and therefore fails to meet all of the claim limitations set forth by the Applicant.

f. Morgan (U.S. Patent No. 4,980,850) discloses a memory device which calculates the total size, starting point, and ending point of all memories that are connected to the device and implements the memories in parallel. Morgan does not teach a method or equation to partition the memories to specific sizes.

g. Schwartz (U.S. Patent No. 4,468,729) teaches physically discrete parallel memories that are automatically assigned sequential addresses.

Schwartz does not disclose a method to divide the memories or an equation to do so.

h. Miyauchi (U.S. Patent No. 6,272,052) teaches parallel memory devices with sequential memory spaces. Miyauchi also fails to disclose an equation or calculation for partitioning the multiple memories.

i. Though all of these teachings are similar to those claimed by the Applicant, no reasonable combination could be made with prior art of record to meet every limitation of the claim. Namely, the inclusion of the function to determine the size of a quanta in the disclosed memory structure.

j. **As for claim 20,** Ukai teaches all the limitations of claim 14, but he fails to teach a method to partition the memory using the equation as specified by the Applicant.

k. See above allowance for claim 1 for other pertinent art in the allowance of claim 20.

11. Claims 2-5 further limit claim 1 therefore they too are deemed allowable.

Response to Arguments

12. Applicant's arguments filed 05 June 2006 have been fully considered but they are not persuasive.

13. **Regarding Claims 6 and 10,** Applicant contests that Ukai fails to disclose "...a second portion of the plurality of storage devices is accessed at a second hardware memory address adjacent to the first hardware memory address." **However, the limitation of the claim states that the memory addresses are merely adjacent. It does not limit the addresses to be physically adjacent. To further clarify, the Office asserts that the addresses are logically adjacent as cited in Ukai: Figure 38 and Column 9, Lines 53-56.**

14. **Regarding Claims 7 and 11,** Applicant contests that Ukai fails to disclose "...with respectively separate address buses." **As previously stated in the rejection Ukai: Figures 1, 18, 24, and 32 show that four drives are accessed separately using a different bus. Furthermore note that inherently, each bus includes an address control and data lines. To further clarify, a bus is a component that transfers data over a connection.**

15. **Regarding Claim 14,** Applicant contests that Ukai fails to disclose "...accessible via a plurality of modes of access to allow selection among a plurality of predefined memory starting points..." and "...wherein the predefined memory access points occur at intervals of less than a total memory bandwidth." **As previously stated in the rejection the "plurality of modes of access" is demonstrated by the read and write functionality of the disk drives disclosed in Ukai. To further clarify, read and write commands are different modes of access therefore demonstrating a plurality of modes of access.**

The write operation allows selection when the disk drive to perform the present write request is selected. The disk is selected in a way that the prior write request will not interfere with running both requests in parallel. It should also be noted that the different disk drives are allocated into a plurality of memory banks. By being able to write to and select each bank it demonstrates the capability of selection.

A "plurality of predefined memory access starting points" is shown in the plurality of banks shown in Figure 37. In column 4, lines 48-53 Ukai states that it is possible to read all of the drives that are connected in parallel. This would then mean that the total memory bandwidth of the system is, in this embodiment, five blocks and the predefined starting points occur every block, therefore occurring at intervals that are less than the total memory bandwidth.

16. **Regarding Claim 19(originally Claim 18),** Applicant contests that Ukai fails to disclose "...wherein the amount of desired data is stored contiguously within a system memory address space of the memory system." **As previously stated in the rejection the reference shows that the blocks are allocated in a contiguous fashion and that data would be stored in that manner. To further clarify, the limitation of the claim is that the data is stored contiguously. The data as taught is stored logically contiguous and therefore meets the limitation.**

17. **Regarding Claims 8 and 12,** Applicant contests that Ukai and Yokote fail to disclose "...the larger storage device comprising an input to select an addressing mode." **As stated in the previous rejection Yokote discloses a controller/memory**

module that is a memory controller, which controls an array of DRAM chips. The controller has multiple input buses in order to determine the location and type of memory access to occur. The controller is able to process read and write instructions, and thereby fulfills the requirement of multiple addressing modes. To further clarify, given that there are multiple addressing modes, read and write, and an input which processes the instructions, an input to select an addressing mode is inherent.

Furthermore, Applicant contests that given the historical differences in properties of "disk drives" and "controller/memory modules" (e.g., capacities), replacing the disk drives of Ukai with the controller/memory modules of Yokote could be expected to lower the storage capacity. **However, the Office will point out that in Yokote: Column 1, Lines 34-50 it is disclosed that the controller/memory modules of the system provide high density and large capacity similar to that of hard disks while also providing the low latency times required by the system. Therefore, combining the controller/memory modules of Yokote with the storage system of Ukai would not be expected to lower the storage capacity.**

18. **Regarding Claim 9 and 13,** Applicant contests that Ukai and Yokote fail to disclose "...wherein the addressing mode allows selection of different hardware memory addresses among the plurality of storage devices for a same memory access operation." **As previously stated in the rejection Yokote discloses the memory controller containing multiple buses, which provide multiple access modes to access memory. Included in these buses are a read data bus, a read address bus,**

a write data bus, a write address, and a control bus. The read address bus and the write address are both capable of handling references to memory addresses, therefore allowing selection of different hardware memory addresses.

The controller/memory modules have the ability to access, in parallel, multiple DRAM chips in the 8x4 array. Accessing in parallel is accessing multiple memories concurrently, in other words, in one memory access operation.

Regarding the contention that there is insufficient motivation to combine Ukai and Yokote see the explanation provided for Claim 8 above.

19. **Regarding Claim 17,** Applicant contests that Ukai and Yokote fail to disclose "...wherein the predefined memory access starting points occur in the memory banks as a function of a size of a desired data block to be accessed." **As previously stated in the rejection Yokote discloses a system that can be configured to accommodate any required storage size. Yokote also discloses the use of an asynchronous transfer mode (ATM). When using an asynchronous transfer mode, data is transferred in units called cells. The cells are of fixed size and format. Although not explicitly stated, the Examiner respectfully asserts that the system Yokote teaches is designed to utilize ATM cells, and therefore is designed to accommodate the usage of a storage unit of ATM cell size. To further clarify, with a cell that has a fixed size and format the system will inherently have predefined memory access starting points that occur as a function of the cell size.**

Regarding the contention that there is insufficient motivation to combine Ukai and Yokote see the explanation provided for Claim 8 above.

20. **Regarding Claim 18(originally Claim 19),** Applicant contests that Ukai and Yokote fail to disclose "...wherein the amount of desired data is an asynchronous transfer mode (ATM) cell." **As previously stated in the rejection Yokote teaches the use of an asynchronous transfer mode (ATM) switch. The use of an ATM switch would imply the use of an asynchronous transfer mode. In the use of an asynchronous transfer mode the data is stored in units called cells. These ATM cells are of fixed size and format. Therefore, although not explicitly stated, the Examiner respectfully asserts that the use of an ATM switch includes the use of an asynchronous transfer mode and an ATM cell.**

Regarding the contention that there is insufficient motivation to combine Ukai and Yokote see the explanation provided for Claim 8 above.

21. **Regarding Claim 16,** Applicant contests that Ukai, McClure, and Koutsoures fail to disclose "...wherein the total memory bandwidth is equal to the burst size." **As previously stated in the rejection Koutsoures refers to setting the cache line length equal to the burst size. The cache line length would be the total memory bandwidth because the memory system cannot transfer more data than the cache line can transfer.**

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within

TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

23. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael B. McFadden whose telephone number is (571)272-8013. The examiner can normally be reached on Monday-Friday 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Manorama Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Mano Padmanabhan 8/21/06

MANO PADMANABHAN
SUPERVISORY PATENT EXAM...

MBM
08/09/2006